

C-7  
Comp  
Sub  
E1  
82.(New) A method according to claim 74 wherein said  
annealing step is conducted by a heating.--

---

REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

The pending claims stand rejected under 35 U.S.C. 102(e) as allegedly being anticipated by Makita '974. However, it is respectfully suggested that Makita '974 is not prior art. Makita '974 has a filing date of September 22, 1997. This is after the U.S. filing date of the present application and specifically March 22, 1996. For these reasons, it is respectfully suggested that the rejection does not meet the Patent Office's burden of providing a *prima facie* showing of unpatentability. It is therefore respectfully suggested that the rejection should be withdrawn.

New claims are also added in order to define additional aspects of the present invention.

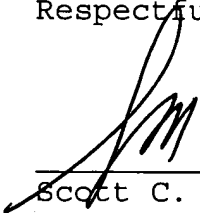
In view of the above amendments and remarks, therefore, all of the claims should be in condition for allowance. A formal notice to that effect is respectfully solicited.

Please apply any charges or credits to Deposit Account

No. 06-1050.

Respectfully submitted,

Date: 8-8-01

  
\_\_\_\_\_  
Scott C. Harris  
Reg. No. 32,030

SCH/smr

Fish & Richardson P.C.  
PTO Customer No. 20985  
4350 La Jolla Village Drive, Suite 500  
San Diego, CA 92122  
Telephone: (858) 678-5070  
Facsimile: (858) 678-5099

10126898.doc

VERSION TO CHANGES MADE

In the Claims:

The claims have been amended as follows.

1. (Amended) A method of manufacturing a semiconductor device comprising the steps of:

forming a crystalline semiconductor film on an insulating surface;

forming an insulating film on said crystalline semiconductor film;

introducing a dopant impurity into said crystalline semiconductor film through said insulating film by an ion doping; and

annealing said crystalline semiconductor film,

wherein a peak of a concentration profile of said dopant impurity is located in said insulating film.

5. (Amended) A method according to claim 1 wherein said crystalline semiconductor film comprises polycrystalline silicon.

22. (Amended) A method of manufacturing a semiconductor device comprising the steps of:

forming a crystalline semiconductor film on an insulating surface;

forming an insulating film on said crystalline semiconductor film;

introducing a dopant impurity into said crystalline semiconductor film through said insulating film by an ion doping; and

annealing said crystalline semiconductor film,  
wherein a peak of a concentration profile of said dopant impurity is located above said insulating surface.

26. (Amended) A method according to claim 22 wherein said crystalline semiconductor film comprises polycrystalline silicon.

43. (Amended) A method of manufacturing a semiconductor device comprising the steps of:

forming a crystalline semiconductor film having a portion to become a channel region on an insulating surface;

forming an insulating film on said crystalline semiconductor film;

introducing a dopant impurity into at least said portion through said insulating film by an ion doping; and

annealing said crystalline semiconductor film,

wherein a peak of a concentration profile of said dopant impurity is located in said insulating film.

52.(Amended) A method of manufacturing a semiconductor device comprising the steps of:

forming a crystalline semiconductor film having a portion to become a channel region on an insulating surface;

forming an insulating film on said crystalline semiconductor film;

introducing a dopant impurity into at least said portion through said insulating film by an ion doping; and

annealing said crystalline semiconductor film,

wherein a peak of a concentration profile of said dopant impurity is located above said insulating surface.